Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Current Sense**
2. **Inverting Input**
3. **Non-Invert Input**
4. **V Ref**
5. **VEE**
6. **VZ**
7. **VO**
8. **VC**
9. **VCC**
10. **Compensation**
11. **Current Limit**

**.044”**

**3 2 1**

**4**

**5**

**6**

**7**

**11**

**10**

**9**

**8**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .044” X .055” DATE: 10/7/21**

**MFG: MOTOROLA THICKNESS .000” P/N: LM723**

**DG 10.1.2**

#### Rev B, 7/1